Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A method of manufacturing an integrated circuit having trench isolation regions in a substrate including germanium, the method comprising:

forming a mask layer above the substrate;

selectively etching the mask layer to form apertures associated with locations of the trench isolation regions;

forming trenches in the substrate at the locations;

providing a semiconductor or metal layer by selective epitaxial growth; and

forming oxide liners using the semiconductor or metal layer in the trenches of the substrate.

2. (Original) The method of claim 1, further comprising providing an insulative material in the trenches to form the trench isolation regions.

3. (Original) The method of claim 2, further comprising removing the insulative material until the mask layer is reached.

4. (Original) The method of claim 1, further comprising:

providing a low temperature process oxide layer above the substrate and an amorphous capping layer above the oxide layer.

5. (Original) The method of claim 1, wherein the amorphous capping layer is amorphous silicon.

6. (Original) The method of claim 1, wherein the semiconductor or metal layer includes silicon material.

7. (Original) The method of claim 1, further comprising:

providing a silicon nitride layer above the substrate and providing an amorphous capping layer above the silicon nitride layer.

8. (Original) The method of claim 1, wherein the forming oxide liners step is an oxidation process.

9. (Currently Amended) A method of forming shallow trench isolation regions in a strained semiconductor layer, the method comprising:

providing a hard mask layer above the semiconductor layer;

providing a photoresist layer above the hard mask layer;

selectively removing portions of the photoresist layer at locations in a photolithographic process;

removing the hard mask layer at the locations;

forming trenches in the hard mask layer under the locations;

providing a conformal semiconductor layer in the trenches by selective epitaxial growth; and

oxidizing to form a liner in the trenches.

10. (Original) The method of claim 9, further comprising:

providing a pad oxide layer above a strained silicon layer before the providing a hard mask layer step.

11. (Original) The method of claim 10 further comprising:

removing the pad oxide layer at the locations before the forming trenches step.

12. (Original) The method of claim 9, further comprising:

providing an insulative material in the trenches to form the shallow trench isolation regions; and

removing the hard mask layer in a wet bath.

13. (Original) The method of claim 9, further comprising:

providing a germanium-containing layer above the strained semiconductor layer.

14. (Original) The method of claim 13, wherein the strained semiconductor layer is at least 200 Å thick.

15. (Original) The method of claim 14, wherein the germanium-containing cap layer is 100 Å –400 Å .

16. (Original) The method of claim 15, wherein the oxide liner is silicon dioxide grown in an oxygen atmosphere.

17. (Currently Amended) A method of forming a liner in a trench in a germanium containing layer, the method comprising:

selectively etching the germanium containing layer to form the trench;

providing a semiconductor layer in the trench by selective epitaxial growth; and

forming an oxide liner from the semiconductor layer.

18. (Currently Amended) The method of claim 17, wherein the ~~semiconductor layer is provided by epitaxial growth, the~~ epitaxial growth ~~bears a deposition process~~ is performed at a temperature below 600C.

19. (Currently Amended) The method of claim 17, wherein the semiconductor layer is provided ~~in a epitaxy process, a chemical vapor deposition process or~~ by molecular beam epitaxy.

20. (Original) The method of claim 19, wherein the oxide liner is 100-200 Å thick.